BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

and the description thereof on pages 6 and 7. No new matter has been introduced into the application.

The Examiner has required additional illustration in regard to positioning of the source and drain regions and damascene connections. This requirement is respectfully traversed since it is believed that these features are well-illustrated in the drawings as originally filed.

In regard to the spatial positioning of the source and drain regions, the Examiner has noted the reference in the specification to these regions being in front and in back of the plane of the page *in cross-sectional drawings*. This is, in fact, the case in regard to cross-sectional drawings of Figures 1 - 5. However, Figures 1A - 5A are *plan* views of the transistor in accordance with the invention and the source and drain regions are clearly illustrated at the left and right sides of each of these figures (e.g. the vertical portions of the "H" shape of the transistor or serifs of the "I" shape of the transistor as referenced in paragraph 0025). In Figures 4A and 5A, in particular, the source and drain regions are the portions of the transistor outside the rectangular areas indicated as the WSiX etch mask and which defines the claimed recess of the gate therefrom.

In regard to the damascene connections, it is respectfully submitted that such terminology is well-understood in the art to refer to conductors formed such as to be supported laterally by material. The term derives from a technique in which a groove or recess in a surface is filled by providing a layer of material which is then patterned by removal of the layer (e.g. by polishing) to the original surface leaving the material in the groove. This structure and technique are well-described in paragraph 0030. Such a structure is well illustrated in Figures 5 and 5A where connection 50 is formed below the surface of the

nitride and the outline of the recesses for source, drain and gate connections are clearly shown and which define the extent of the damascene connections.

Accordingly, it is seen that the subject matter for which the Examiner has required additional illustration is already clearly illustrated in the drawings as originally filed. Therefore, reconsideration and withdrawal of this requirement is respectfully requested.

Claim 1 has been rejected under 35U.S.C. §112, second paragraph, as being indefinite; the Examiner criticizing the term "sub-lithographic". This ground of rejection is respectfully traversed.

It is respectfully submitted that the term "sub-lithographic" is a well-recognized term of art connoting that the dimension referenced is not directly determined by lithographic patterning of a mask or resist and that the dimension is smaller than can be resolved by a lithographic exposure using a given tool or design rules (e.g. minimum feature size regime). Since improvements in lithographic resolution allow scaling of devices to smaller sizes and some features of integrated circuit elements are defined as to size and location by lithographic exposure, "sub-lithographic" is clearly an apt expression to convey a relative dimension as well as being a well-recognized and well-understood term of art. Therefore, it is respectfully submitted that the term "sub-lithographic" is not, in fact, subject to being "interpreted in various ways" and that no ambiguity or lack of clarity as to claim scope or impediment to determination thereof is presented by use of the term and reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claims 4, 5, 7 and 8 have been rejected under 35 U.S.C. §112, first paragraph, as being drawn to subject matter which is not supported by enabling disclosure in

regard to damascene connections. This ground of rejection is also respectfully traversed.

As discussed above in connection with the drawings, damascene connections are well-known and well-understood in the art. Damascene connections are formed by "by lithographically defining and etching openings in the STI material at appropriate locations and depositing metal in the openings and on the surface as shown at 50 of Figure 5", as explicitly recited in paragraph 0030. This summary of the damascene process is entirely sufficient to enable damascene connections to be made without undue experimentation even if damascene connections and the process for making them were not well-known and well-understood in the art. Since damascene connections are, in fact, well-known and well-understood in the art, even this description of the technique of their formation is unnecessary to enablement of the successful practice of the invention by persons skilled in the art. Therefore, it is respectfully submitted that this ground of rejection is clearly in error and reconsideration and withdrawal of the same is respectfully requested.

Claims 1 - 3 have been rejected under 35 U.S.C. §103 as being unpatentable over Mizuno et al. in view of Sung and claims 4 - 8 have been rejected under 35 U.S.C. §103 as being unpatentable over Mizuno et al. in view of Sung and Liu et al. These grounds of rejection are respectfully traversed.

Mizuno et al. is directed to formation of a transistor at small size and improving the turn-off characteristics thereof and thus superficially resembles the invention is several respects such as formation of a gate structure which partially surrounds the conduction channel. However, Mizuno et al. does not teach or suggest formation of the conduction channel to have a sub-lithographic width preferably achieved by undercutting of a mask as illustrated in

Figure 2 (which supports the particularly improved turn-off characteristics of the transistor in accordance with the invention since the distance over which the gate must control the conduction of the channel is reduced - the channel of Mizuno et al. is clearly defined lithographically and thus cannot be sub-lithographic), a gate structure which is recessed from the source and drain regions (which supports the reduction of gate capacitance as noted in paragraph 0028 - Mizuno et al. forms source and drain regions in a "self-matched" (e.g. self-aligned) manner using the gate as a mask as noted at column 8, lines 15 - 32 such that the gate is contiguous with the source and drain regions), or silicide sidewalls on the source drain *and* gate (which supports reduction of resistance of these elements). Particularly in combination, these features of the invention provide further improvement in performance and electrical characteristics while being capable of manufacture at smaller size than the transistor of Mizuno et al. Only the last of these three clear deficiencies of Mizuno et al. is recognized by the Examiner.

These deficiencies of Mizuno et al. to answer the claimed subject matter are not remedied by Sung and/or Liu et al. Sung is cited by the Examiner for teaching silicide spacers 8. However, column 3, lines 56 and 60 clearly identify these spacers as being tungsten and the description of their formation does not suggest silicidation. Liu et al. is cited for teaching formation of damascene interconnects which is correct but does not teach or suggest any other of the claimed features noted above which are not taught or suggested by Mizuno et al. Since the statements of the rejections are silent as to the features of sub-lithographic channel width and recessing of the transistor gate from the source and drain and incorrect in regard to the provision of silicide, especially on

all of the gate, source and drain, the Examiner has failed to make a *prima facie* demonstration of obviousness of any claim in the application. By the same token, the references do not provide evidence of a level of ordinary skill in the art which would support the conclusion of obviousness that the Examiner has asserted, particularly since they do not lead to an expectation of success in deriving the meritorious effects of the invention such as further improved electrical characteristics at smaller sizes. Further, the stated grounds of rejection are clearly in error in failing to consider express recitations of the claims such as those noted above as well as failing to determine the level of ordinary skill in the art (e.g. the teaching of damascene connections in Liu et al. clearly indicates the impropriety of the rejections under 35U.S.C. §112, first paragraph, or recognition of the well-understood term "sub-lithographic". Rather, the Examiner has used clearly improper rejections under 35 U.S.C. §112 to buttress rejections based on prior art which does not answer the express recitations of the claims.

Accordingly, it is respectfully submitted that the stated grounds of rejection are in error and untenable, particularly as the claims have been further clarified by amendment. Therefore, reconsideration and withdrawal of the rejections based on prior art is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such

APPENDIX

Paragraph 0021:

The SOI wafer, as described above will generally include a thick so-called handling wafer or substrate 10 covered by a buried oxide (BOX) 12. Monocrystalline semiconductor layer 14, in turn, covers the buried oxide 12. Doping levels are relatively low in the preferred embodiment of this device, with the requirement that the channel be fully depleted. Typical doping levels are preferably in the [1015/cm3 to 1017/cm3] $\underline{10^{15}/cm^3 \text{ to } 10^{17}/cm^3}$ range with the high $10^{16}/cm^3$ range being preferred. The process of the present invention begins by forming a layer of pad nitride of about 100 nm thickness and a pad oxide of about 3 - 10 nm thickness over the silicon and patterning the nitride using a patterned resist 18. The silicon height will determine device width and is preferably in the range of 50-200 nm. Many suitable resists and lithographic techniques for patterning them are familiar to those skilled in the art and specifics thereof are unimportant to the practice of the invention.

Claim 1:

1. (Amended) A field effect transistor comprising

a conduction channel of sub-lithographic width,

source and drain regions <u>located at opposite ends of said conduction channel, said source and drain regions</u> having silicide sidewalls on a surface thereof, and

polysilicon gate regions on opposing sides of said conduction channel <u>and recessed from said source and drain regions</u>, said polysilicon <u>gate regions</u> having silicide sidewalls formed thereon [and recessed from said source and drain regions].

action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,

Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P. C.
11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190

(703) 787-9400